CLAIMS

What is claimed is:

1. An memory IC comprising:

a first group of banks of memory having a first bank, a first row address decoder coupled to the first bank, and a first bank selection logic coupled to the first row address decoder;

a second group of banks of memory having a second bank, a second row address decoder coupled to the second bank, and a second bank selection logic coupled to the second row address decoder, all able to operate independently of the first bank, first row address decoder and first bank selection logic;

control logic shared by both the first and second groups, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first group, including the first bank, and separately storing information concerning the state of all banks in the second group, including the second bank; and

a data buffer shared by both the first and second groups.

2. The memory IC of claim 1, wherein the control logic and the data buffer cooperate to couple the memory IC to a memory bus and share access to the memory bus between the first and second groups, with the control logic receiving at least addresses and commands from the memory bus for memory operations involving both the first and second groups, and with the data buffer transferring data between the memory bus and both the first and second groups.

3. The memory IC of claim 2, wherein the control logic incorporates logic to arbitrate between the first and second groups for access to the data buffer to transfer data to and from the memory bus.

4. The memory IC of claim 1, wherein the control logic stores information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

5. The memory IC of claim 1, wherein a read transaction to read data from a row within the first bank is able to be timed and carried entirely independently of a read transaction to read data from a row within the second bank.

6. An electronic system comprising:

a memory IC having a first group of banks having a first bank, second group of banks having a second bank, control logic shared by both the first and second groups and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group, and a data buffer;

a memory controller having a third state logic storing information concerning the state of all banks in the first group within the memory IC, and having a fourth state logic storing information concerning the state of all banks in the second group within the memory IC; and

a memory bus coupling the control logic and data buffer of the memory IC to the memory controller.

7. The electronic system of claim 6, wherein the control logic and the data buffer cooperate to share access to the memory bus between the first and second groups, with the control logic receiving at least addresses and commands from the memory bus for memory operations involving both the first and second groups, and with the data buffer transferring data between the memory bus and both the first and second groups.

8. The electronic system of claim 7, wherein the control logic incorporates logic to arbitrate between the first and second groups for access to the data buffer to transfer data to and from the memory bus.

9. The electronic system of claim 6, further comprising

a processor coupled to the memory controller; and

a cache utilized by the processor to store a subset of data stored in the memory IC.

10. The electronic system of claim 9, wherein the memory controller incorporates a control storage to maintain information concerning the size of a cache line within the cache.

11. The electronic system of claim 6, wherein the control logic stores information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

12. The electronic system of claim 6, wherein the control logic permits a read transaction to read data from a row within the first bank is able to be timed and carried entirely independently of a read transaction to read data from a row within the second bank.

13. The electronic system of claim 12, wherein the memory controller transmits addresses and commands to the memory IC for a first read transaction to read data from a first row within a bank in the first group and for second read transaction to read data from a second row within a bank in the second group, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction, wherein the memory controller times the first and second read transactions to minimize the time that elapses between the end of the actual transfer of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction.

14. The electronic system of claim 13, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early through indications of early termination embedded in the commands transmitted to the memory IC for both the first and second read transactions.

15. The electronic system of claim 13, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early through transmitting first and second burst termination commands across the memory bus, timed to indicate when to cease transferring further bytes of data for each of the first and second read transactions.

16. A method comprising:

selecting a first read operation to read data from a first row in a first group of banks in a memory IC;

selecting a second read operation to read data from a second row in a second group of banks in the memory IC;

determining a quantity of bytes to which each transfer of data will be limited for both the first and second read operations;

transmitting a first read command for the first read operation to the memory IC;

waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the end of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation;

transmitting a second read command for the second read operation to the memory IC;

receiving the burst transfer of data for the first read operation from the first row of the first group; and

receiving the burst transfer of data for the second read operation from the second row of the second group.

17. The method of claim 16, further comprising checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

18. The method of claim 16, further comprising signaling the memory IC that both the first and second read operations are to be terminated early through indications of early termination embedded in the commands transmitted to the memory IC for both the first and second read operations.

19. The method of claim 16, further comprising signaling the memory IC that both the first and second read operations are to be terminated early through transmitting first and second burst termination commands to the memory device, timed to indicate when to cease transferring further bytes of data for each of the first and second read operations.

20. A machine-accessible medium comprising code that when executed by a processor within an electronic system, causes the electronic system to:

interrogate a memory device to determine whether or not the memory device possesses banks of memory cells organized into a plurality of groups that permit independent memory operations;

configure a memory controller to make use of a memory device that possesses such independently operable groups of banks of memory cells;

check the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in a memory device that possesses such independently operable groups of banks of memory cells; and

determine a quantity of bytes to which to limit the burst transfer of bytes of data in a read transaction from a memory device that possesses such independently operable groups of banks of memory cells.